JPL’s Thermal Testing Philosophy

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JPL’s Mission

- JPL is an operating division of the California Institute of Technology & is a Federally Funded Research & Development Center (FFRDC)

- JPL’s primary mission, performed under contact to NASA, is the robotic exploration of the solar system; for example
  - Mars Scouts 2007, Mars Reconnaissance Orbiter, Mars Exploration Rover, Mars Odyssey, Mars Global Surveyor
  - Deep Impact, Dawn, Stardust, Genesis
  - Galileo, Cassini, Ulysses, Voyager

- JPL also has significant involvement with NASA programs in Earth Sciences & Astrophysics
  - TOPEX/Poseidon, Jason, Jason 2, GRACE, CloudSAT
  - NSCAT, QuikSCAT, SeaWinds, MLS, MISR, AIRS, TES
  - SIR-C, SRTM
  - SIM, SIRTF, GALEX, WF/PC on HST, IRAS
Overview of JPL’s Products & Processes

- Develop Hardware Products Process
- Design Product Systems Process
- System Thermal Test Standard

Hardware Assemblies

Subsystems (Instrument and/or Spacecraft)

Thermal Engineering & Flight System Thermal Control Procedure

Flight System (Instrument and/or Spacecraft)

Environmental Testing Procedure
JPL’s Thermal Testing Philosophy for Thermal Design Purposes

• JPL uses early thermal development testing in the thermal design evolution cycle to proactively develop robust designs
  – Empirically determine key driving thermal parameters that are difficulty to quantify analytically
  – Understand temperature sensitivity to key boundary conditions
  – Demonstrate proof-of-concept

• System thermal testing serves multiple objectives
  – Empirically validate system-level thermal design for thermally extreme conditions
  – Validate flight system functionality under flight-like environmental conditions
    · Include verification of flight thermal hardware such as electrical heaters with mechanical thermostats, temperature sensors, heat pipes, etc.
  – Gather test data for analytical thermal model correlation
    · Calibrated tool for “Verification by Analysis”
JPL’s Thermal Testing Philosophy for Hardware Products

• JPL uses protoflight (PF)/qualification (QUAL) to uncover workmanship defects & vulnerable design features
  – Interplanetary flight systems require high reliability since their in-flight duration may be several years
  – These types of missions experience minimal thermal cycling
    • Thermal cycles are limited on flight hardware to 33% of expected ground + flight
    • Dwell times at hot or cold soak test cases protracted to ensure reliability
  – Earth-orbiting & Mars-surface missions experience more pronounced thermal cycling
    • Hardware packaging must demonstrate life cycling to 3 times expected flight (packaging verification qualification)
    • Non-compliance requires a Project waiver
      › One-time or limited use items (e.g., deployment mechanisms)
  – Typically, these tests are conducted in vacuum (< 10^{-5} torr)
• Flight acceptance (FA) testing used to certify hardware whose design has undergone QUAL testing
<table>
<thead>
<tr>
<th>TYPE OF THERMAL TEST</th>
<th>GOVERNING DOCUMENT</th>
<th>INTERNAL JPL DOCUMENT ID</th>
</tr>
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<tbody>
<tr>
<td>System or Flight</td>
<td>System Thermal Testing Standard</td>
<td>58172</td>
</tr>
<tr>
<td>Assembly Level</td>
<td>Design Product Systems Process</td>
<td>57354</td>
</tr>
<tr>
<td>Thermal Balance</td>
<td>Environmental Testing Procedure, Revision 3</td>
<td>33832</td>
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<tr>
<td>Flight Assembly</td>
<td>Assembly and Subsystem Level</td>
<td>60133</td>
</tr>
<tr>
<td>PF/QUA/FA</td>
<td>Environmental Verification Standard</td>
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<tr>
<td></td>
<td>Develop Hardware Products Process</td>
<td>57752</td>
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<td>Environmental Testing Procedure, Revision 3</td>
<td>33832</td>
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<td>Thermal Development</td>
<td>Thermal Engineering and Flight System</td>
<td></td>
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<tr>
<td></td>
<td>Thermal Control Procedure, Revision 1</td>
<td>33014</td>
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<td>Environmental Testing Procedure, Revision 3</td>
<td>33832</td>
</tr>
</tbody>
</table>
Typical Thermal Testing Flow

PDR ▼

CDR ▼

ATLO START ▼

FS SHIP ▼

LAUNCH ▼

THERMAL DEVELOPMENT TESTING

SYSTEM THERMAL TESTING

ASSEMBLY PF/QUAL/FA TESTING
Environmental Requirements Are Mission-Unique

- JPL Design Principles recommend specific temperature margins & thermal cycling

- Each project develops an “Environmental Requirements Document (ERD)”
  - Captures Design Principles as the baseline
  - Provides for tailoring based on such criteria as critical functionality & lifetime
  - Prescribes mission-unique specifications for temperature margin between allowable flight temperature (AFT) & test levels (PF/QUAL/FA), PF/QUAL/FA dwell times, & number of thermal cycles
• System-level thermal testing enables validation of flight thermal hardware
  – Primary & secondary heater strings including thermostats, if any
  – Heater power margin
    · General guideline is a maximum 75% duty cycle in the worst-cold case
  – Temperature sensor measurements comparison to test thermocouple readings
  – Heat pipe/CPL start-up

• Steady-state criteria
  – Each flight system responds differently
  – Prescribing a temperature rate of change or heat flow criteria is arbitrary without incorporating specific thermal characteristics
  – While JPL specifies a temperature rate of change, steady-state determination is left to the discretion of the test conductor
    · If the steady-state temperatures can be credibly extrapolated from test data, then a test case can be considered “steady”
Thermal Design Validation Considerations (2/3)

<table>
<thead>
<tr>
<th>Test Characteristic</th>
<th>Thermal Development</th>
<th>System or Flight Assembly Thermal Balance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Thermal Cycles</td>
<td>Not applicable if no flight hardware used</td>
<td>Minimized since thermal cycling is considered a limited &amp; consumable resource</td>
</tr>
<tr>
<td>Dwell Time</td>
<td>Sufficient for steady-state determination</td>
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<tr>
<td>Temperature Range</td>
<td>Allowable flight temperature (AFT)</td>
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## Thermal Design Validation Considerations (3/3)

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<td>Temperature Extremes</td>
<td>Not to exceed a known material limit and/or safe condition if no flight hardware used</td>
<td>Not to exceed FA</td>
</tr>
<tr>
<td>Transition Rate</td>
<td>Not to exceed a known material limit and/or safe condition if no flight hardware used</td>
<td>Not to exceed a safe hardware condition; Limiting items include optics (&lt;8°C/hr)</td>
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<tr>
<td>Thermal Stability</td>
<td>&lt;0.3°C for 3 consecutive hours or at discretion of cognizant test conductor</td>
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## Hardware Certification Considerations

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<tr>
<td><strong>Number of Thermal Cycles</strong></td>
<td>Flight assemblies: Typically 3 to 10 cycles</td>
</tr>
<tr>
<td></td>
<td>Packaging: 3 times worst-case flight</td>
</tr>
<tr>
<td><strong>Dwell Time</strong></td>
<td>Tailored on a unique Project basis, Typically 144 hours HOT &amp; 24 hours COLD</td>
</tr>
<tr>
<td><strong>Temperature Range</strong></td>
<td>PF/QUAL: AFT - 15°C to AFT + 20°C (Electronics shall minimally be -35 to +75°C)</td>
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### Cassini STV Test Phase 1 Event Timeline

**Event Timeline Chart**

<table>
<thead>
<tr>
<th>Event No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>S/C Baseline Test</td>
</tr>
<tr>
<td>2</td>
<td>Close Chamber</td>
</tr>
<tr>
<td>3</td>
<td>Nitrogen Flush</td>
</tr>
<tr>
<td>4</td>
<td>Start Cooling Shrouds</td>
</tr>
<tr>
<td>5</td>
<td>Turn OFF Purge</td>
</tr>
<tr>
<td>6</td>
<td>Configure Power for Case 1A</td>
</tr>
<tr>
<td>7</td>
<td>Turn off Heaters TBD for Cooldown Acceleration</td>
</tr>
<tr>
<td>8</td>
<td>Configure Power for Case 1B</td>
</tr>
<tr>
<td>9</td>
<td>CIRS Interference Test</td>
</tr>
<tr>
<td>10</td>
<td>CAPS HV Test</td>
</tr>
<tr>
<td>11</td>
<td>CDA Interference Test</td>
</tr>
<tr>
<td>12</td>
<td>ISS Interference Test</td>
</tr>
<tr>
<td>13</td>
<td>Radar 30 minute Turn-ON</td>
</tr>
<tr>
<td>14</td>
<td>RWA 30 minute Turn-ON</td>
</tr>
<tr>
<td>15</td>
<td>Turn on Heaters for warm-up acceleration</td>
</tr>
<tr>
<td>16</td>
<td>Configure Power for Case 1C</td>
</tr>
<tr>
<td>17</td>
<td>CIRS, VIMS &amp; ISS Functional Tests and CIRS Microphonics Test</td>
</tr>
<tr>
<td>18</td>
<td>Configure Power for Backfill turn ON Purge</td>
</tr>
</tbody>
</table>

**Diagram Notes**

- Ambient
- Soak
- Hot (Case 1A)
- Cold (Case 1B)
- Cold (Case 1C)

**Temperature (oC)**

-40 -30 -20 0 20 40 60 80 100 120 140 160

**Test Time (Hours)**

- 0 2.7 0 0.5
MER IPA SN001
PF Thermal Vacuum Test Profile

3 thermal cycles with 50 & 24 cumulative hours hot & cold, respectively

1 hour hold @ HOT & COLD
Start at least once at each plateau

Temperature

Time
Case Study – Electronics Box

- An externally mounted power distribution box (PDB)
  - Nominal power dissipation: 36 watts
  - Safe mode power: 8 watts
  - AFT limits:
    - Op: -20 to 45°C
    - Survival: -20 to 50°C
  - Predicted temperature range:
    - -5 to 34°C for a 5-year low-earth orbit mission (EOL optical properties & dissipation)
  - Requires thermostatic heaters to maintain PDB at or above -15°C
    - Thermostat setpoints: -15 & -5C
    - Powered on survival bus operating between 24 & 32V
Primary & backup survival heater strings that have both power switches enabled

AFT limits apply to the bulk average temperature

Primary & backup thermostats setpoints staggered

No heat flow allowed through mounting I/F

Radiator area probably needed, provisions in place to permit easy area modification

Insulation covers entire unit except for radiator area

Heater power < 24W (current draw < 1 amp, only series thermostats required)
Hardware Design Assumptions (1/2)

• Assume PF test program
  – PF operating test levels: -35 (cold) & 70°C (hot)
    • Driven outside −15/+20°C margin to meet minimum of −35 to 70°C
    • 3 to 10 thermal cycles
    • Dwell cumulative 24 hrs cold & 144 hrs hot
    • Assume a temperature ramp rate of 120°C/hr is acceptable
  – PF survival test levels: no cold test required, covered by operational test
    • Unit “turn-on” at non-operating levels captured by PF operating test
  – Assume hardware can fit into 3-foot diameter thermal vacuum chamber

• Assume electronics packaging qualification successful
  – Assume 2 cycles a day for 5 years = 3650 flight cycles
  – Assume ground testing adds additional 6 thermal cycles
  – 3 times life = 10,968 thermal cycles
Hardware Design Assumptions (2/2)

Assume PDB thermal design is straightforward; No thermal development testing required.
PF Testing

- PF testing accomplished by mounting flight hardware to a heat exchanger & using chamber shroud
  - PDB will be covered with a test thermal blanket

- If multiple units were fabricated (i.e., flight spare), these units could be tested to FA levels upon concurrence from QA
  - FA operating levels: -25 to 50°C
  - FA dwell times: 24 hrs cold & 50 hrs hot
  - FA number of thermal cycles: probably 3
System Thermal Test (1/2)

• Validate PDB power dissipation
  – Obtain copy of Hardware Requirements & Certification Review (HRCR) power sheet
  – Verify power dissipation with PDB ATLO engineer
• Establish extreme thermal test conditions
  – Internal power & external environment
• Determine if any special PDB tests are required
  – Primary & secondary heater string validation
  – Consider power sensitivity for radiator sizing
  – Empirical data for verification by analysis
• Determine if PDB needs a test heater
  – EOL heat load simulation
  – Acceleration, warm-up, fail-safe and/or special test requirements
• Determine PDB test instrumentation locations
System Thermal Test (2/2)

- Establish test yellow & red alarms
  - Yellow: AFT limits
  - Red: FA levels

- Understand & accommodate ATLO’s functional test needs for the PDB
  - Review end-to-end functionality V & V rather than focusing on temperature requirements
  - Determine need for any special test targets or support equipment

- Develop contingency plans in the event the design is deficient
References


