THERMAL ANALYSIS OF A LASER COMMUNICATIONS NETWORK INTERFACE CARD USING THE ICEPAK SOFTWARE

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ABSTRACT

Swales Aerospace, under contract from Space Photonics, Incorporated, has performed board level thermal analysis of a four channel, optical network interface card (NIC) from SPI's FireRing® product line. The FireRing® NIC is a laser communications module with a total aggregate bandwidth of 10.0 Gbps – 2.5 Gbps per channel. The development of this product line has been made possible by various SBIR contracts and private DOD contracts supported by NASA-GSFC, NASA-JPL, and AFRL-Kirtland. The NIC is a primary component within the overall Intelligent Node Optical Communications Architecture that has been under development at SPI for the past seven years. The work performed under this contract is helping to prepare the Intelligent Node Optical Communications System for space qualification and to discover thermal and mechanical challenges related to space flight before they become issues. Since this work is concurrent with much of the system architecture design, quick turnarounds and ease of modification and presentation were required. Thus, the software chosen for the thermal analysis was Fluent's IcePak. IcePak is primarily used in the terrestrial electronics industry; therefore, some special considerations were necessary when analyzing boards in space applications. Presented here are the methods and results from the analysis of the FireRing® Network Interface Card (NIC) using the IcePak software.

INTRODUCTION

This paper discusses the methodology used to perform thermal analysis on a prototype board design implementing new technologies that have yet to be flown in space. The board is a network interface card (FireRing® NIC) that contains fiber optic receive and transmit modules (FireFiber® MP4-2500RX and MP4-2500TX).

Icepak was chosen as the software in which to analyze this board. This software is typically used for terrestrial board and box level thermal analysis. It is capable of complex CFD solutions, radiation analysis, and solid conduction. For this effort, the CFD and radiation capabilities of the software were turned off and only conduction heat transfer was used. Icepak also has easily implemented tools for modeling boards which made it the software of choice for this task over other software.

BACKGROUND

The Intelligent Node program is an effort funded primarily by the Air Force Research Lab (AFRL-Kirtland) via a Phase III DoD contract. This development effort is being executed by Space Photonics, Inc. of Fayetteville, AR to develop and qualify a complete inter-satellite fiber optic interface (FOI) and intra-satellite gimbal-less free space optical (FSO) communications system for harsh environment terrestrial and space-based applications.

SPI has contracted Swales Aerospace to perform mechanical and thermal design and analysis tasks to guidepost the efforts of the program. This will help insure the design and subsequent hardware will be ready for space qualification.

The FOI portion of the Intelligent Node System is divided into two major subsystems: the fiber optic transceiver set and the network interface card itself. The transceiver subsystem will be an optical assembly and housing that will be externally mounted to the spacecraft in several locations to provide the required field of view. The network interface is a card designed to be internally mounted, most likely in a C&DH box. The NIC provides data translation services from the copper domain to the optical domain, routes the optical data to the transceiver, and retranslates the data back to the copper domain.

This paper focuses solely on the NIC thermal analysis efforts.

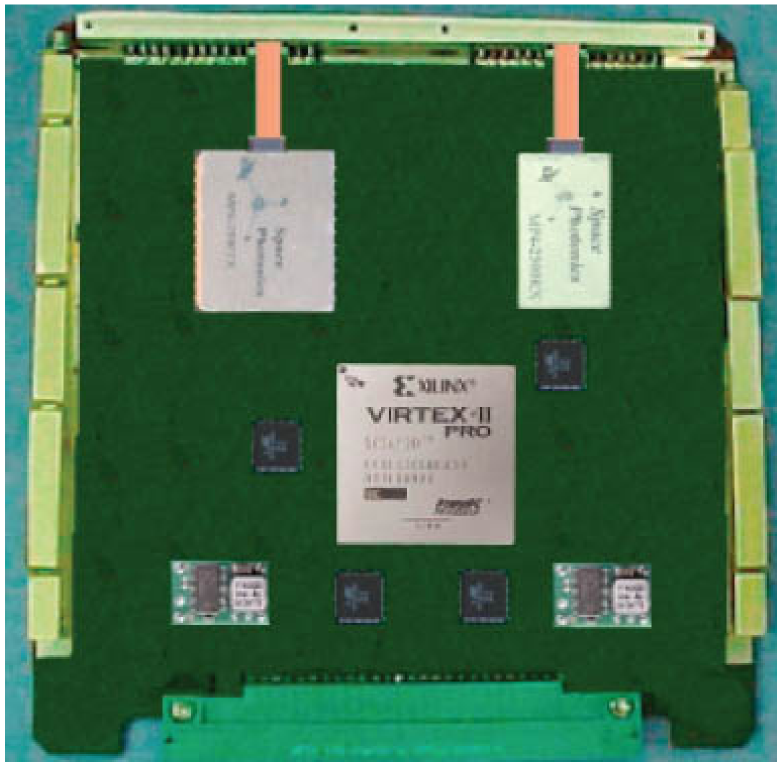

Figure 1: Early Generation FOI NIC Prototype

Figure 2: First Generation FSO Transceiver Prototype

NIC DESIGN DETAILS

The NIC was designed around the SEM-E architecture standard. The board footprint was established at 5.88”X6.06”. An overall thickness of .093” was assumed. The board was modeled as a 10 layer board, with signal and ground planes consisting of 2.0oz-Cu. The board was assumed to be retained by a standard Wedge-Lock.

The board contains two components, in addition to the board itself, manufactured by Space Photonics: a fiber optic laser transmitter and a receiver (FireFiber® MP4-2500RX and MP4-2500TX). The current design of these devices enables operation of up to four channels simultaneously; therefore, as a worst case scenario, all analyses were performed assuming steady state operation with all four channels powered.

Three iterations of the design were analyzed. The first iteration was very simplistic with only seven components modeled. Component placement was driven solely by optimizing thermal performance from which SPI based the initial layout. Complexity and simulation accuracy increased as the design and modeling process evolved. This first iteration established the mounting methods required for some of the components. The second and third iterations were based upon the actual, evolving board layouts.

METHODOLOGY

In order to force Icepak to give reliable solutions for solid state conduction while neglecting convection and radiation, certain parameters required manipulation. The first set of parameters are found under the Basic Parameters dialog. Figure 3 shows the setup used for Basic Parameters. Only steady state is selected and the only variables solved are temperatures. Radiation is turned off.

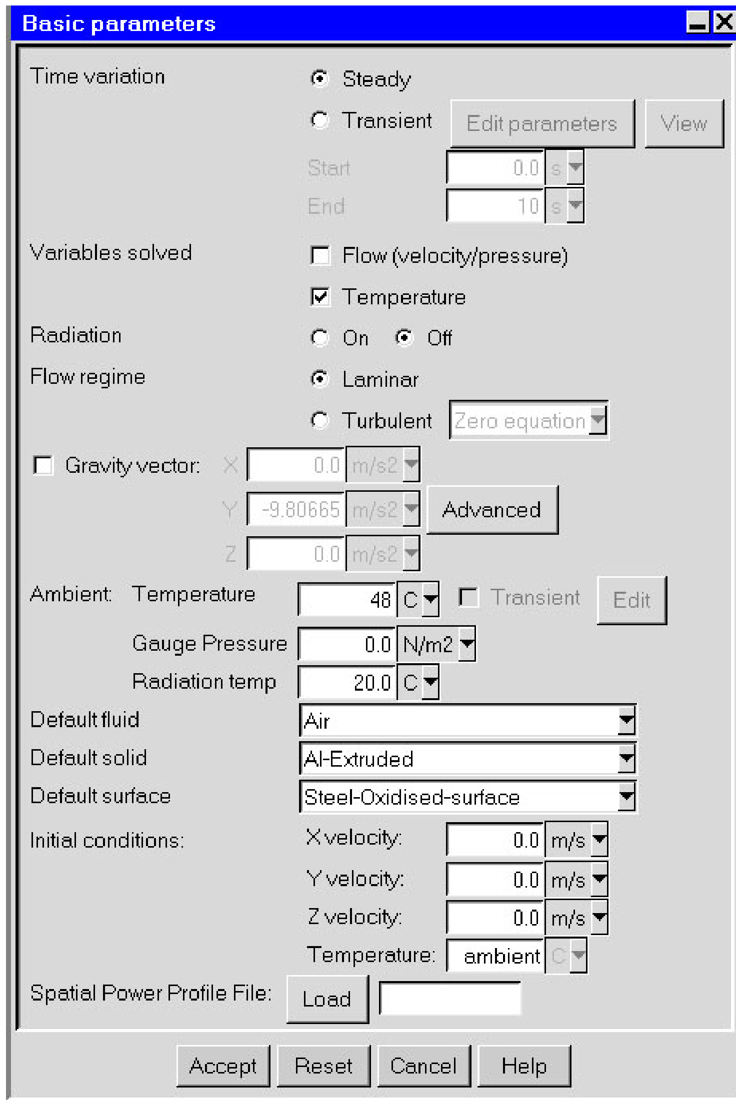

Figure 3: IcePak Basic Parameters

Note that since radiation is neglected, the surface properties are not used by the program.

Icepak bounds board level problems by the use of a "cabinet" entity. The cabinet defines not only the volume used for airflow but also boundary temperatures and external heat loads or losses. For this problem, the cabinet was eliminated. This, coupled with turning off the flow

solution in the Basic Parameters, forces a solid conduction only solution. In order to disable the cabinet, the cabinet geometry shape must be set to "None" as shown in Figure 4.

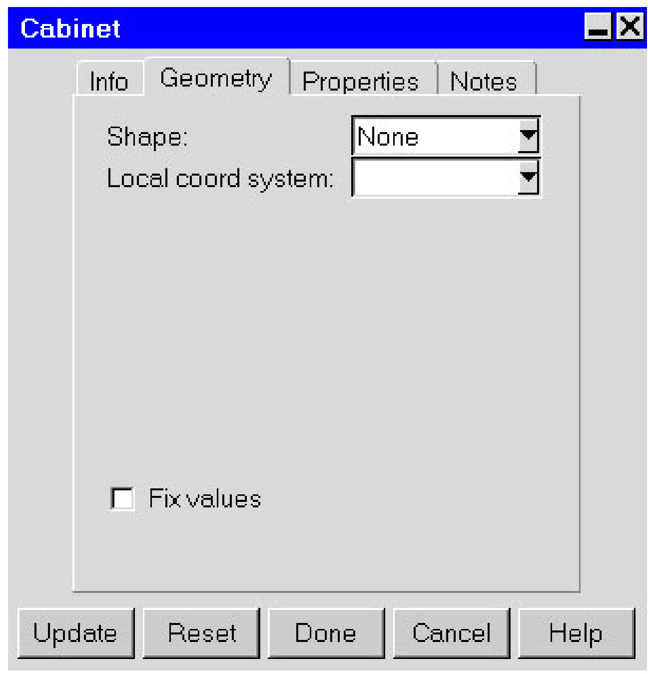

Figure 4: IcePak Cabinet Parameters

Finally, some Advanced Solution Parameters must be changed from the default. The temperature solution method should be changed to type "W" with a termination criteria of 1e-6 and residual reduction tolerance of 1e-6. The precision should also be changed to double precision. This is shown in Figure 5. These parameter changes were suggested by Fluent to improve the solution when only calculating temperatures.

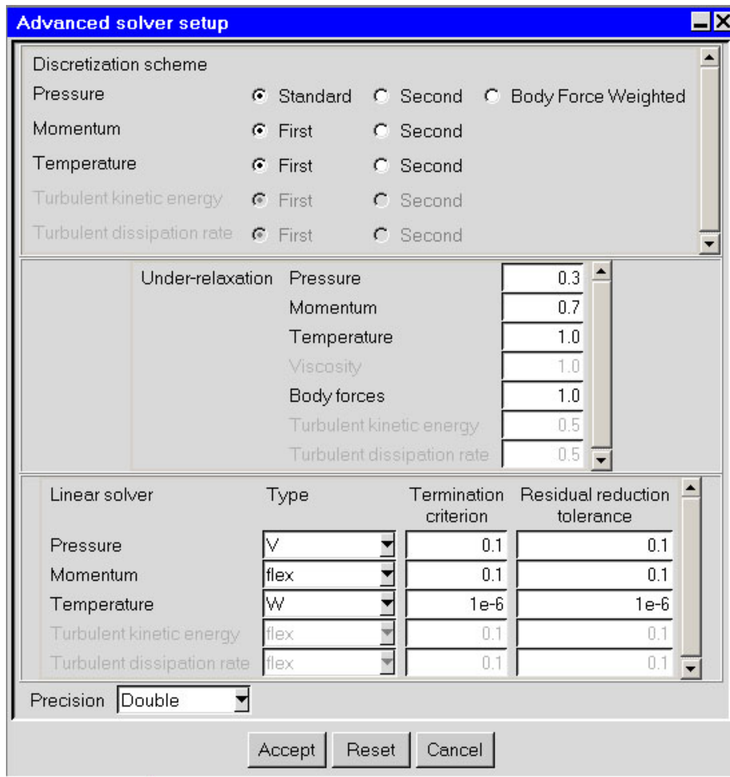

Figure 5: IcePak Advancer Solver Parameters

In most board level analyses, the package temperature is calculated out to a junction temperature by factoring in the manufacturer's measured Θj-c value. However, in this analysis, the Θj-c was unknown for most components so EEE-INST-002 derated junction temperature limit for the component type was further derated for comparison to package temperatures. While this approach would not be advisable for flight configuration analysis, it was deemed adequate due to the technology development nature of this program. The conservatisms applied throughout the modeling make risk of later redesign minimal.

For the analysis, boundary conditions were established at the wedge-locks by placing a constant temperature wall element stacked on top of the card guide block. A plate element was placed between the card guide block and the PCB block. The plate acts as the interface conduction. It was assigned a contact resistance factor of 0.4534 °C/W. This value was calculated from the cross section of the wedge-lock card guide geometry. The card guide boundary temperatures were set at 65°C and 55°C. These boundary conditions were derived from Solar Dynamics Observatory board analysis requirements. When an actual flight is determined, these boundary temperatures will be revisited and reduced if practical.

Each component was modeled as a block with arbitrary material properties. This can be done because the heat load is uniformly applied to the entire package so no gradients in the package are modeled. A plate element was sandwiched between the package block and the PCB to act as the conductance path. The resistance from each package to PCB was calculated separately and included a combination of contact and package lead conduction factors. Attempts were made to manage thermal dissipation via package leads alone but typically required some thermal

interface – primarily leaded active devices. Some components do not have package leads but instead have solder terminations. In the later case, a solder thickness of 1mm with a fill factor of 95% was assumed. In practice, the solder thickness will be considerably thinner in most places with a maximum thickness of 1mm being possible in very local areas. The solder is assumed to be Type 281 Sn/Pb with a conductivity of 0.19W/cm-K. All package leads were assumed to be gold plated Kovar with a conductivity of 0.163W/cm-K.

The second and third iterations contained the Virtex II Pro FPGA with a ball grid array (BGA). Conduction from the BGA was calculated by assuming some dimensions of the solder balls post reflow. In the case of the Virtex, the original dimensions of the solder balls was .6mm OD. It was assumed the solder balls would compress into a cylindrical shape post reflow with dimensions of 0.65mm OD and a height of 0.55mm. Solder 281 Sn/Pb was again assumed.

The PCB is modeled as "compact." This is an IcePak option that reduces the PCB to essentially a one dimensional problem by calculating an effective normal and in-plane conductance based upon layer characteristics. The other option, "detailed" would model each individual layer and result in much higher element counts. For this problem, all internal signal layers were assumed to have a copper coverage of 1% while the top and bottom layers were assumed to have copper coverage of 75%. This results in effective normal conductivity of 0.33W/m-K and in-plane conductivity of 18.1W/m-K.

In some cases, thermal dissipation for components was not well defined for the actual usage on this board. When this was the case, manufacturer's maximum values were used. In addition to this, 1.0W was assumed to be distributed on the PCB to simulate load from resistors and other passives which were not physically modeled.

Table 1 shows the parts list for the third iteration of the board.

Table 1. NIC Parts List with Dissipation

Part Designation	Type	Power Dissipation, W
TX	Laser Transmitter	1.3
RX	Laser Receiver	0.66
VR33A	Step Down Regulator	0.214
VP20	Virtix II FPGA	0.87
VR15A	Voltage Regulator	0.80
VR18A	Voltage Regulator	0.80
VR25A	Voltage Regulator	0.80
AP1A	Voltage Regulator	0.80
AP1B	Voltage Regulator	0.80
O1	Oscillator	0.05
O2	Oscillator	0.05
LA1	Linear Amplifier	0.17
LA2	Linear Amplifier	0.17
LA3	Linear Amplifier	0.17
LA4	Linear Amplifier	0.17
P1	PROM	0.66

RESULTS

The first iteration highlighted the need for certain design changes to improve thermal performance. The Tx and Rx components represented highest dissipation on the board during the first iteration. With only the package leads providing conduction from the board, these components easily exceeded temperature limits. At this time, it was decided to use a thermal interface to conduct heat from these components into the PCB. The chosen interface method was a copper "slug" mounted to the component case with Ablefilm 561k film adhesive. The copper slug is assumed to be 0.8mm thick and pure copper. Ablefilm 561k has a manufacturer's reported thermal conductivity of 0.008W/cm-K. These materials together constitute a thermal impedence between case and board of 0.097°C-cm^2/W. Even after this was added, additional measures were needed. At this time, it was decided to bond an aluminum heat spreader plate to the back of the PCB. Ablefilm 561k was again assumed to be used for this purpose. The aluminum plate was assumed to be 1/16 inch and the card guides were to be mounted to the aluminum plate instead of the PCB. This rectified temperatures of the Tx and Rx and became the baseline design used in further iterations.

The second iteration saw several new components added: voltage regulators, oscillators, and amplifiers as well as the PROM. The voltage regulators and amplifiers were particularly problematic since both have high dissipations and small package footprints.

The third iteration consisted of a layout change only. No new components were added and no dissipations changed. The thermal concerns for the voltage regulators and amplifiers were not fully addressed by this iteration and remain to be investigated.

Temperature results for the third iteration are shown if both Table 2 and Figure 6.

Table 2. Component Temperature Results and Margins, Iteration 3

Part Designation	Type	Case Temp, °C	EEE-INST-002 Derated Temperature Limit, °C	Temperature Margin, °C
TX	Laser Transmitter	79.1	* 80.0	0.9
RX	Laser Receiver	77.9	* 80.0	2.1
VR33A	Step Down Regulator	76.7	100.0	23.3
VP20	Virtix II FPGA	77.6	**80	2.4
VR15A	Voltage Regulator	96.7	100.0	3.3
VR18A	Voltage Regulator	94.9	100.0	5.1
VR25A	Voltage Regulator	96.6	100.0	3.4
AP1A	Voltage Regulator	94.5	100.0	5.5
AP1B	Voltage Regulator	95.5	100.0	4.5
O1	Oscillator	77.0	110.0	33.0
O2	Oscillator	77.7	110.0	32.3
LA1	Linear Amplifier	87.4	***85	-2.4
LA2	Linear Amplifier	87.5	***85	-2.5
LA3	Linear Amplifier	86.8	***85	-1.8
LA4	Linear Amplifier	86.6	***85	-1.6
P1	PROM	90.7	***85	-5.7

All temperature limits are case temperatures backed out from NASA EEE-INST-002 Standard except:
* Part type not defined in EEE-INST-002
** No Theta J-C value, limit is conservative minimum
*** Manufacturer's ambient limit

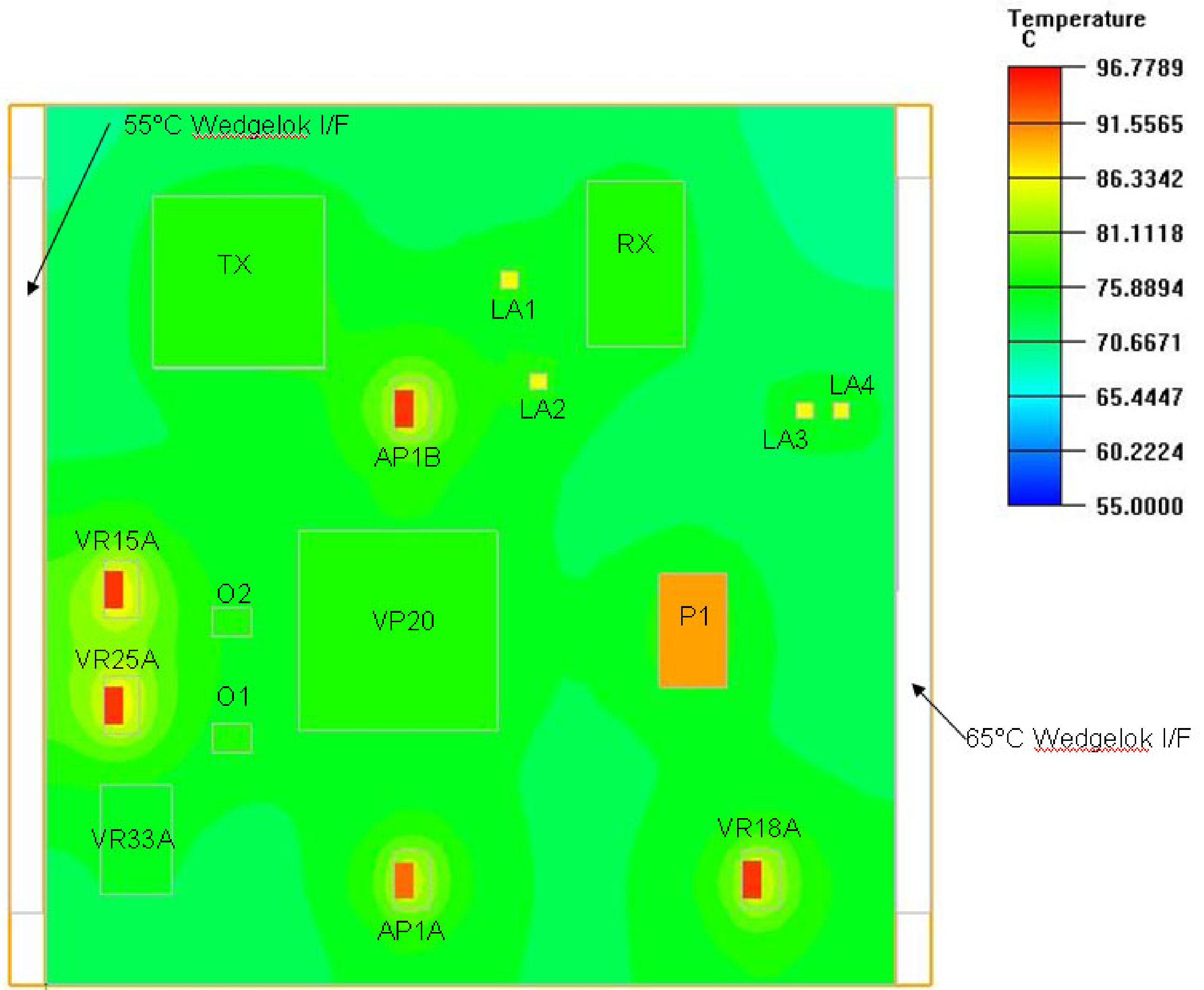

Figure 6: Icepak Temperature Plot for NIC

CONCLUSIONS

While substantial thermal concerns still exist, it is believed that they are completely surmountable. The voltage regulators are actually mounted to the bottom side of the board and thus are tied directly to the ground plane. This also eliminates the possibility of using the aluminum heat spreader plate and may result in other thermal issues in a worst case scenario or conservative simulation. The linear amplifiers will be provided with a solder slug that ties them thermally to the groundplane. The Tx and Rx components are also being provided with this feature. All of these design changes will require a shift in the manner in which the PCB has been modeled.

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NOMENCLATURE, ACRONYMS, ABBREVIATIONS

Θj-c Thermal resistance from device junction to case
CFD Computational Fluid Dynamics
NIC Network Interface Card
FOI Fiber Optic Interface
FPGA Field Programmable Gate Array
FSO Free Space Optical
PCB Printed Circuit Board
PROM Programmable Read-Only Memory
Rx Receive module
SBIR Small Business Innovation and Research
SPI Space Photonics, Inc.
Tx Transmit module
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