Thermal Modeling and Test Correlation for the High Fidelity Data Acquisition System

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MSFC EV34

Presented By
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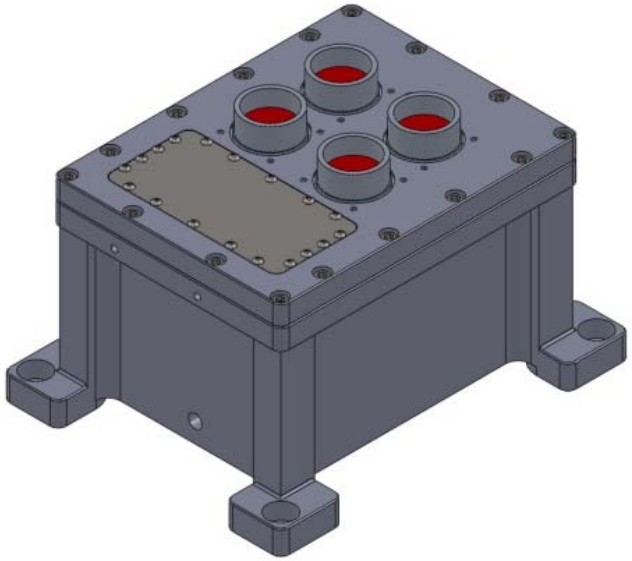
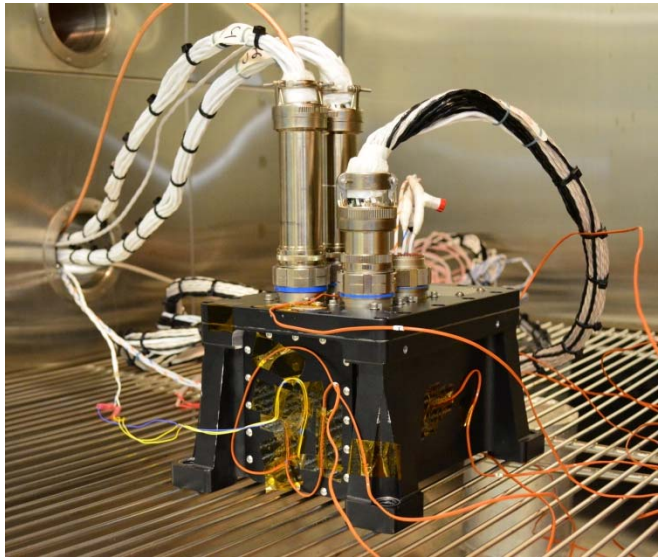
Background



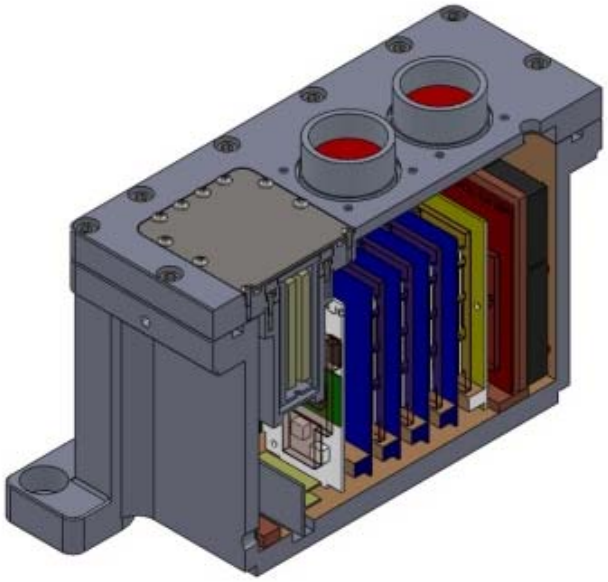


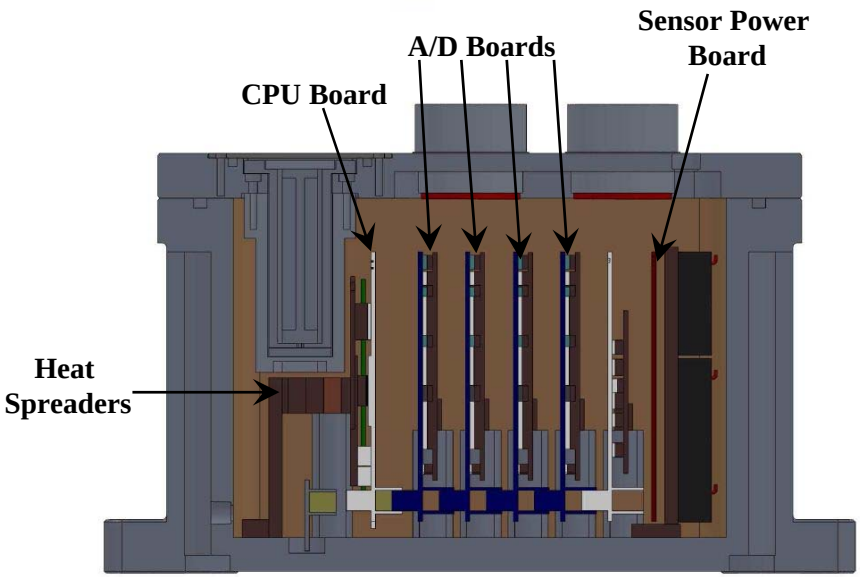
- High Fidelity Data Acquisition System (HiDAQ)
- Compact electronics data recorder for use in high-vibration and potentially high transient heating environments
  - e. g. next to a rocket engine
- Sponsored by NASA Engineering Safety Center (NESC)
  - Vendor was Optical Sciences Corporation
  - Intended for Max Launch Abort System (MLAS)
  - Continued for potential SLS use

Thermal Requirements

Req. Number	Req. Title	Requirement	Verification
3.3.1.1	Continuous Operation Environment	The HiDAQ unit shall be capable of continuous operation in a -10°C to +40°C environment.	Analysis & Test
3.3.1.2	Qualification Temperature Range	The stretch qualification temperature range for the HiDAQ unit shall be 10°C beyond the operating temperature range.	Analysis & Test
3.3.1.3	Chassis Operating Temperature Range	The minimum and maximum operating temperature range for the HiDAQ chassis shall be -20°C to +140°C during a flight operation duration of 10 minutes or less (as stated in Requirement 3.1.2).	Analysis
3.3.1.4	Electrical Piece Part Non-Operating Temperature Range	The minimum and maximum non-operating temperature range for the HiDAQ unit shall be -20°C to +65°C.	Analysis & Test

Hardware Design – Major Components

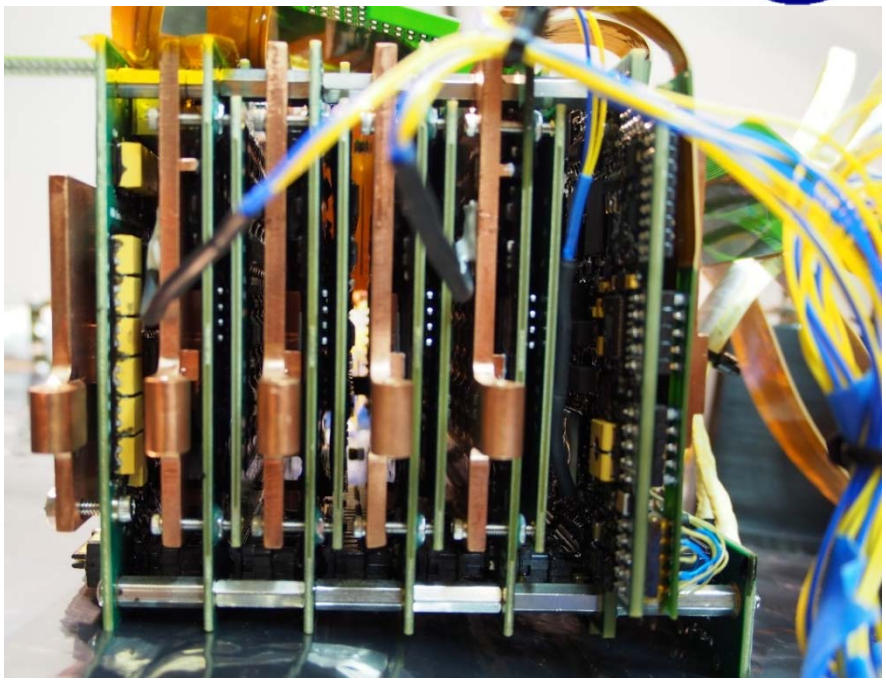




- Aluminum chassis
- 7 main circuit boards, 5 “daughter” boards
- Copper heat spreaders
- 15V Power Supply
- RFI filter
- Solid State Drives (SSDs)
- Remaining space filled with epoxy

Hardware Design - Thermal Management

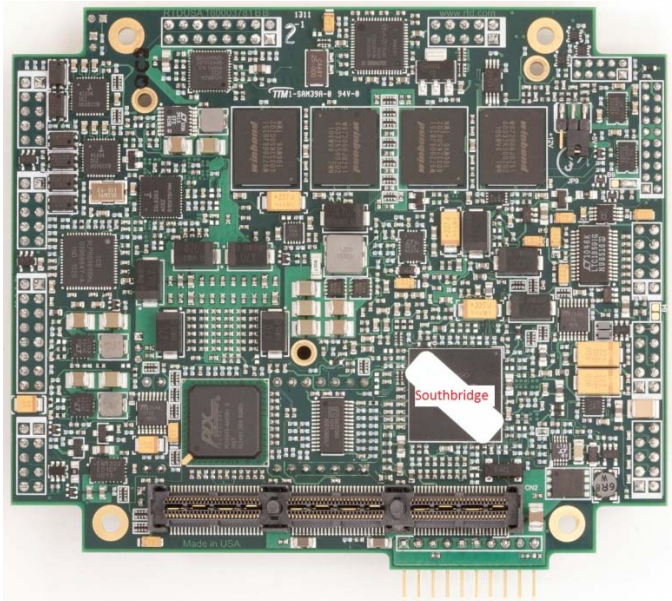
- Heat spreaders
  - Copper plates
  - Contact chips
- Epoxy fill
  - Epoxies Etc. 50-3151 FR
  - Entire box is filled with epoxy
  - Primary purpose is vibration protection
  - “Thermally conductive” epoxy used to provide better heat dissipation
  - Thermal conductivity at 25°C
    - Air k = 0.026 W/m/K
    - Epoxy k = 0.741 W/m/K
    - Aluminum k = 225 W/m/K
    - Circuit Board k = 0.73W/m/K

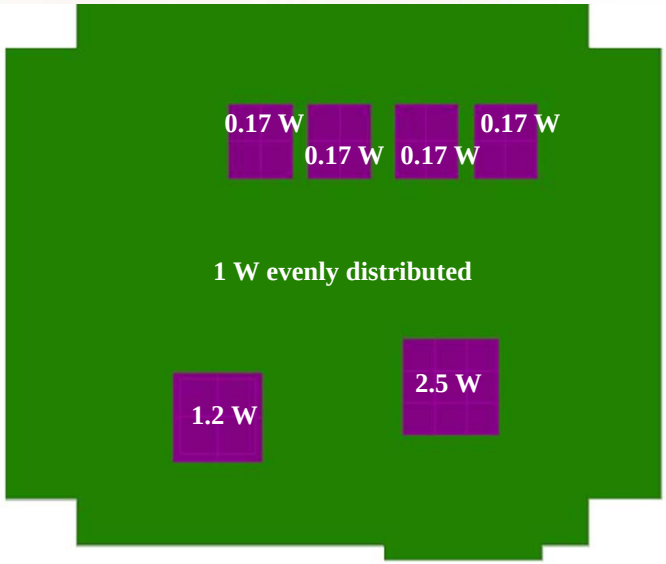


DAQBRICK with epoxy fill

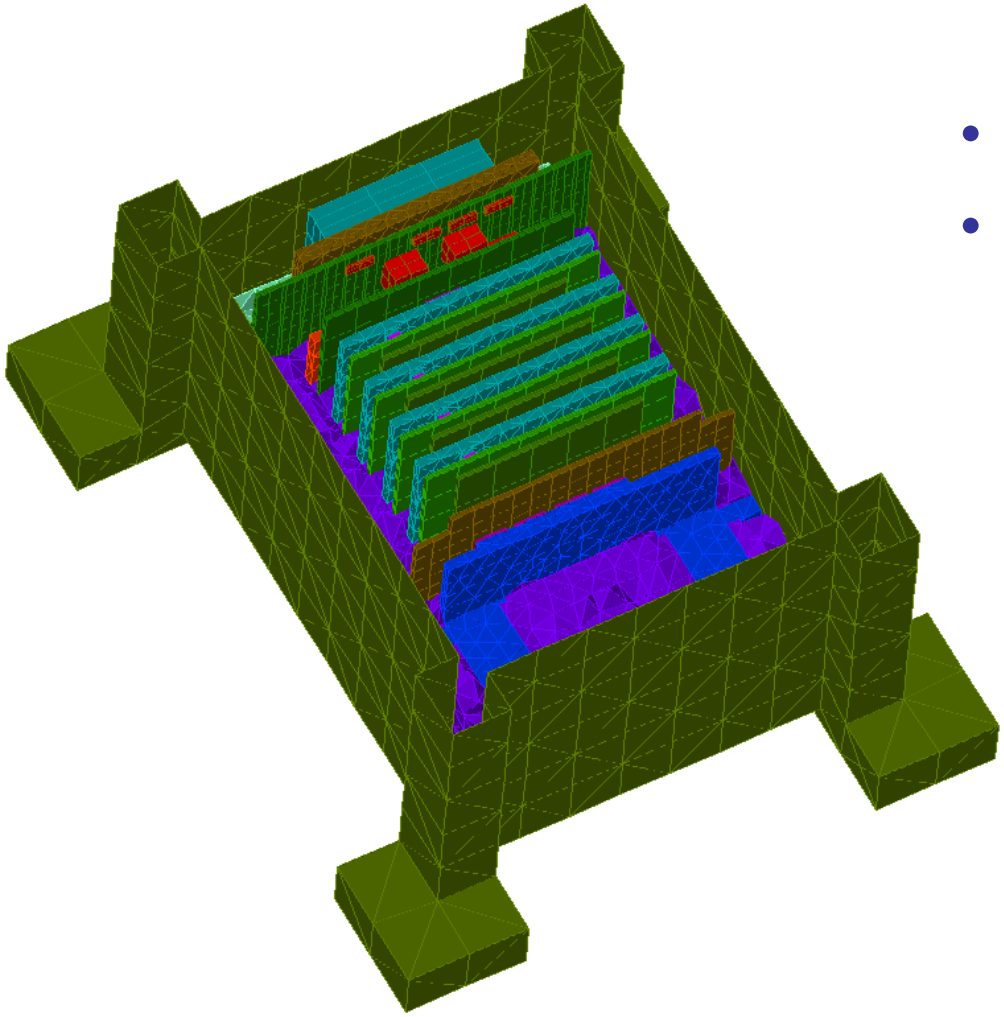
Thermal Model

- Components meshed in FEMAP
- Analysis performed using Thermal Desktop
- Fairly high-detail
  - Enclosures, boards, and heat spreaders fully rendered
  - Individual chips represented to the extent possible
    - Emphasis on largest and highest dissipation chips
- Heat generation
  - Volumetric heat loads on modeled components
  - Distributed heat loads over board surface to capture dissipation of smaller components
- Contactors connect adjacent objects
  - Allow modeling of contact resistances and air gaps



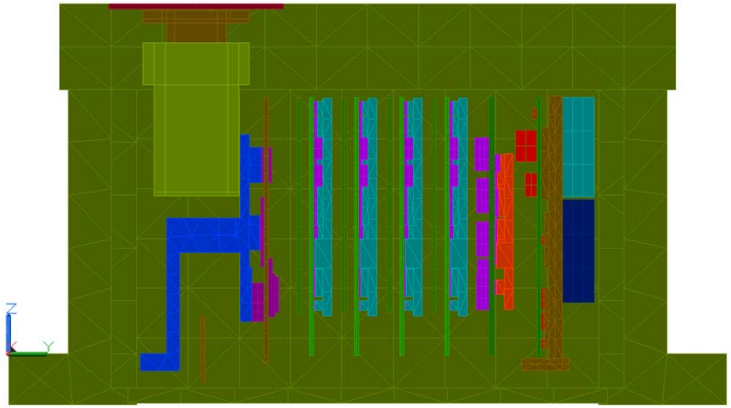


Thermal Model Discretization



Isometric view (top lid and upper epoxy region hidden)

- 27500 nodes
- 75000 solid elements

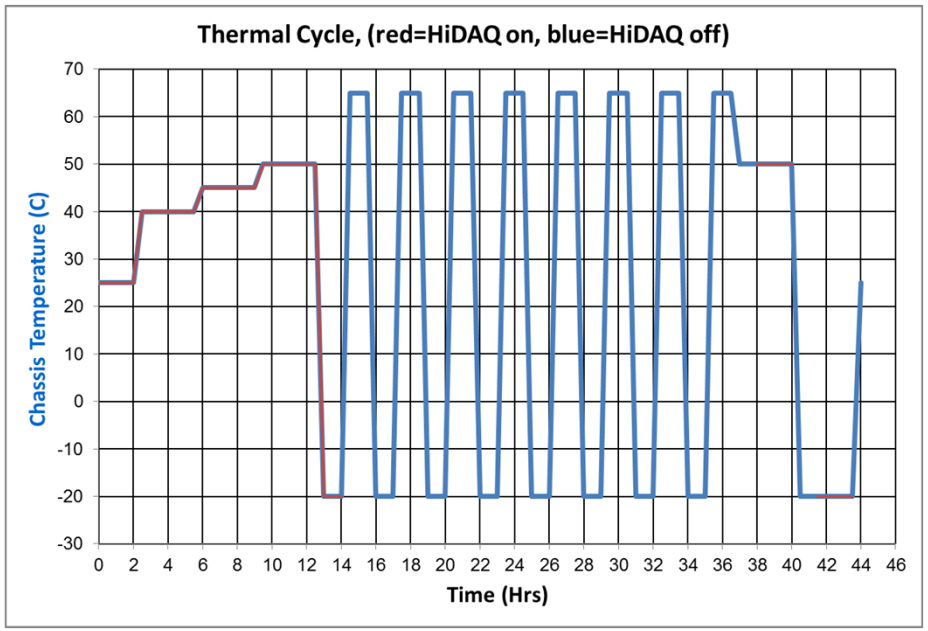


Side view with internal components

Model Assumptions

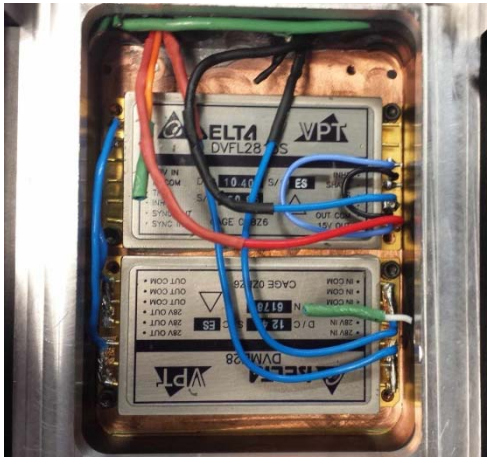
- Electronics components (chips, RFI filter, SSDs) modeled as solid silicon
  - Exception: 15V power supply modeled as epoxy to improve fit
- Conduction only
  - No convection in air spaces
  - No radiation
- Chassis boundary condition: fixed temperature at each surface
  - Surface temperature on each side taken from thermocouple readings in test data
- “Air gap” used to simulate “bubbles” and contact resistance between epoxy and components (initial estimate: 0.01mm gap)
- Negligible losses from wires/cables

Thermal Testing



- Tests
  - Thermal cycling
    - Steady operation at qualification conditions
      - 50°C ambient (hot), -20°C ambient (cold)
  - Transient “hot flight” test
  - Thermal vacuum
- 11 RTD sensors used to record temperatures of major components
  - Generally mounted on top of heat spreaders – not direct chip measurements
- 8 TCs record temperatures on each side of the box and in chamber
- Results used for model correlation to determine optimum values for parameters

Correlation Challenges



- Hardware damage
  - Epoxy from last board to end of box was machined out to replace a component damaged in prior vibration tests, leaving a large void
  - ***Approach: Model geometry, mesh, and contactors remade to include an air void.***
- Uncertain heat loads
  - Power consumption only measured at board level
  - ***Approach: Used spec sheets to obtain estimates of power consumption for highest dissipation chips. Remaining power spread uniformly over board.***
- Sensor issues
  - RTD sensors consistently off by different amounts
  - ***Approach: Unpowered, steady-state readings at known temperatures used to determine individual offsets for each RTD. Data adjusted by these offsets. Transient data used to confirm that offset is consistent and not a random fluctuation.***
- Material properties
  - Limited information from vendor on epoxy thermal properties: no specific heat data, no temperature dependent thermal conductivity data
  - ***Approach: Material properties tested at MSFC. Measured thermal conductivity only ~50% of spec value.***
- "Black boxes"
  - Internal details of RFI filter and 15V power supply unknown
  - ***Approach: Assumed to be solid silicon boxes initially, material choices adjusted to epoxy to improve fit.***

Correlation – Parametric Study

- Epoxy-component contact resistance
  - Modeled as an air gap (initial estimate: 0.01mm gap)
  - Moderate impact
- Thermal paste thickness
  - Epoxy connects chips to spreaders (initial estimate: 0.1mm thick)
  - Moderate impact, but high uncertainty, potentially high variability, and limited reasonable range
- Power distribution
  - High impact, but some uncertainty
- Epoxy properties
  - Resolved through materials testing
- Heat spreader-chassis contact conductance
  - Low impact

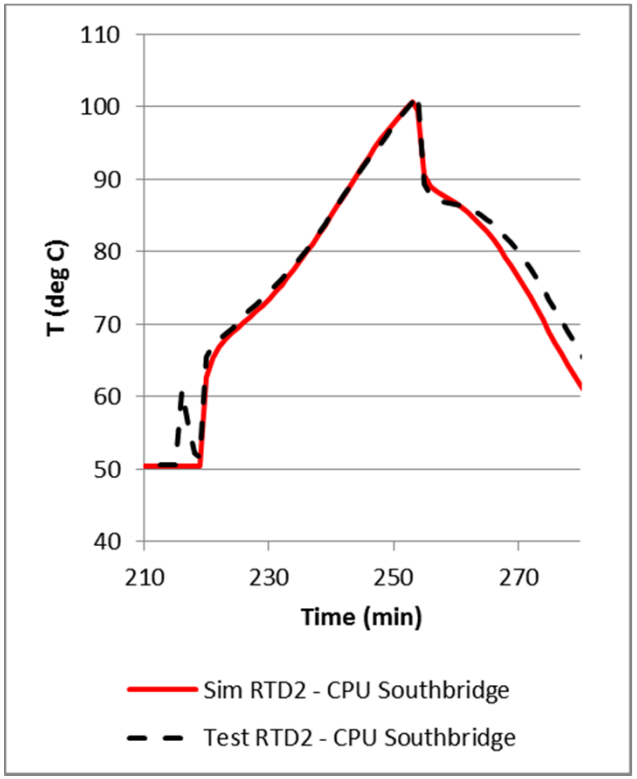
Correlation – Steady-state Results

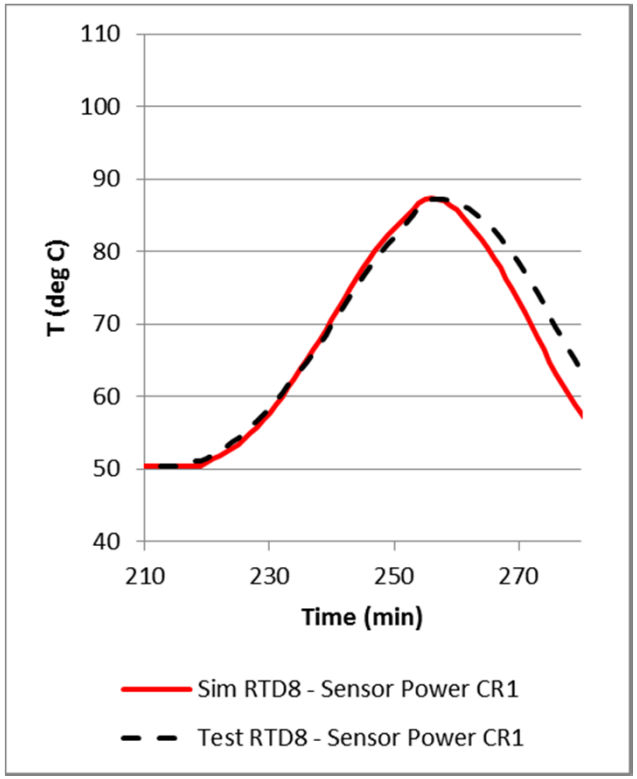
- Temperature results with initial estimates for parameter values
  - Results largely within 5°C of test values
  - Largest temperature deviation on one CPU chip, >10°C off
- Parametric studies showed low sensitivity to most parameters
  - Power distribution has a high impact, but is not known precisely
  - Epoxy contact resistance has a moderate impact
- Model correlation approach
  - Correct largest discrepancies with minor tweaks to a small number of parameters
  - Small tweaks to a few parameters to get in the right range
    - Increased heat load on the high-deviation CPU chip (balanced by reductions on other chips)
    - Epoxy-component "air gap" increased to .02mm
  - Model temperature results within ~5°C of test values, most within ~3°C

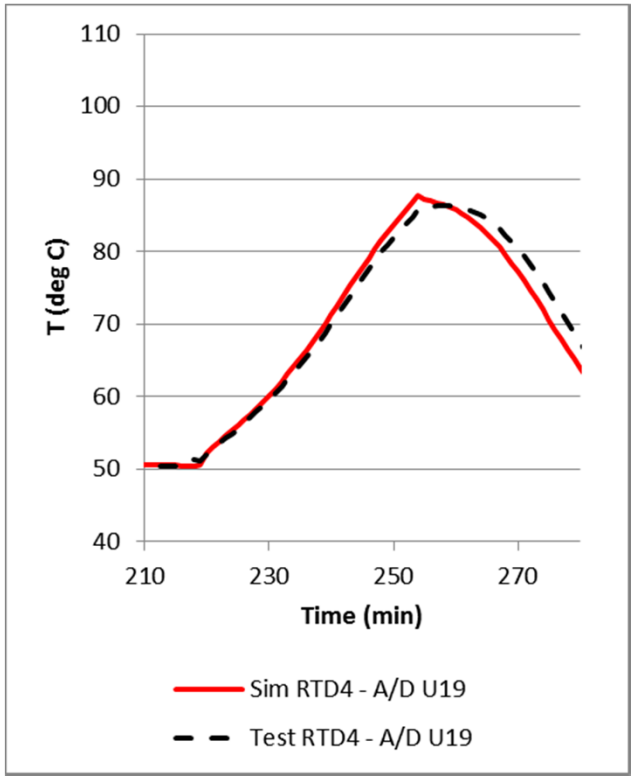
Table: Correlation Results

		Hot Case			Cold Case		
RTD #	RTD Name/Location	Experimental Test Value (deg C)	Initial Sim-Test Error (deg C)	Refined Sim-Test Error (deg C)	Experimental Test Value (deg C)	Initial Sim-Test Error (deg C)	Refined Sim-Test Error (deg C)
1	101 <AD Board 1 Chip U303> (C)	69.2	-2.2	-0.7	-3.5	0.6	2.2
2	102 <CPU Southbridge> (C)	81.9	-11.2	-2.3	8.8	-7.5	2.1
3	103 <AD Board 1 Chip U19> (C)	69.9	-3.3	-1.8	-2.8	-0.6	1.0
4	104 <AD Board 4 Chip U19> (C)	67.9	-1.5	-0.1	-4.3	0.7	2.2
5	105 <Stack Power Board Inductor> (C)	70.8	-3.8	-2.0	-2.3	-0.6	1.3
6	106 <CPU Northbridge> (C)	65.1	-0.7	0.4	-8.9	2.9	4.1
7	107 <Sensor Power Board FWT> (C)	66.1	-5.8	-5.3	-6.5	-4.1	-3.7
8	108 <Sensor Power Board CR1> (C)	64.9	-4.0	-3.3	-7.9	-2.0	-1.4
9	109 <AD Board 4 U303> (C)	67.6	-0.7	0.7	-5.0	1.8	3.3
10	110 <CPU Intel CPU Chip> (C)	64.8	-0.9	0.0	-9.0	2.4	3.3
11	111 <DCDC Converter> (C)	66.3	0.2	2.3	-4.1	0.9	3.3

Correlation – Transient Results





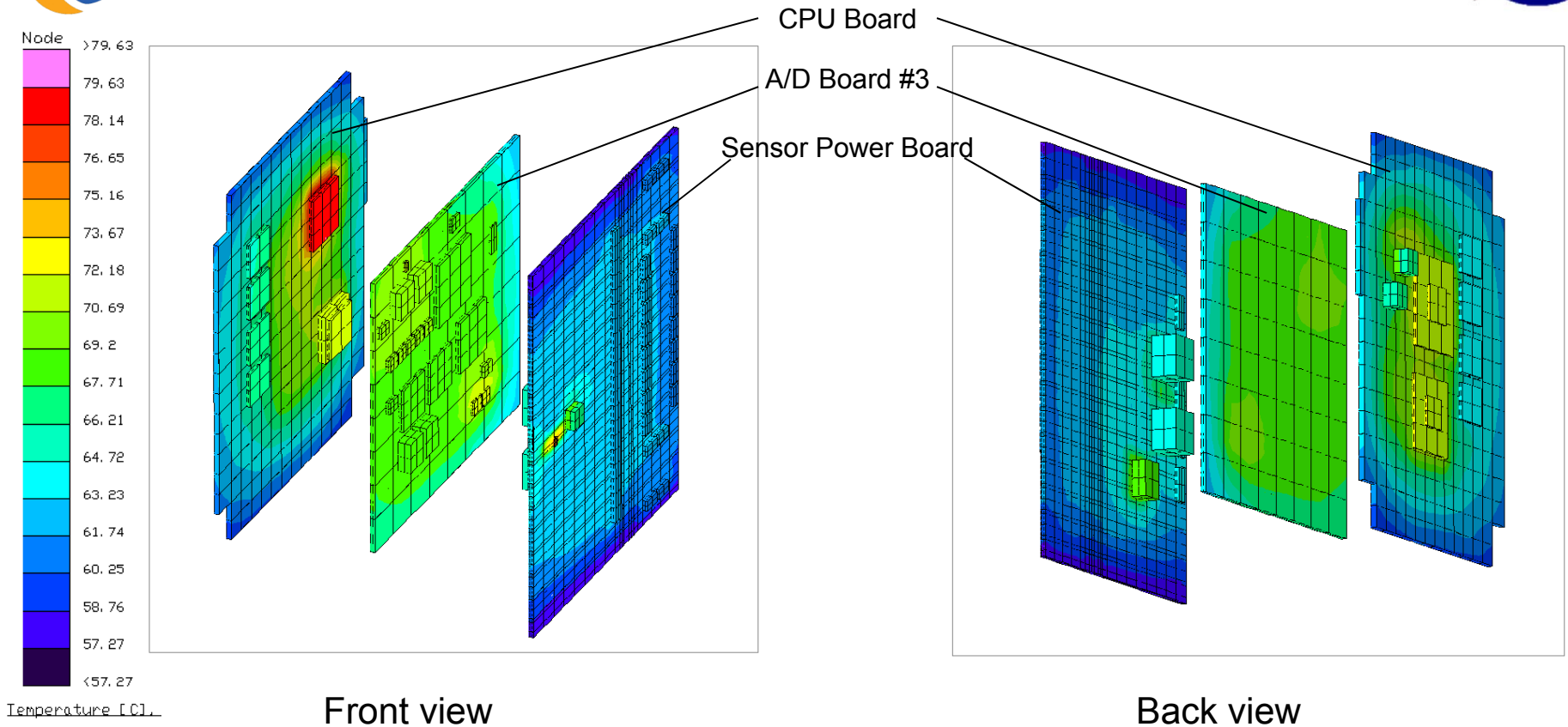


- "Hot flight test" ramped chamber temperature up from 50°C to 90°C, until Southbridge CPU reached 100°C
- Simulation with refined parameters also shows good agreement in a transient case

Simulation Results – Nominal Operation

- Model was correlated to the test configuration
  - Test unit was damaged during vibration testing
    - Test article did not have power to all boards
    - Test article had some epoxy removed at one end of the box
- After parameter values were refined through correlation, simulations were conducted for situations representing an “as designed” box
  - Box completely filled with epoxy
  - All boards on

Simulation Results – "As Designed" Model



Front view

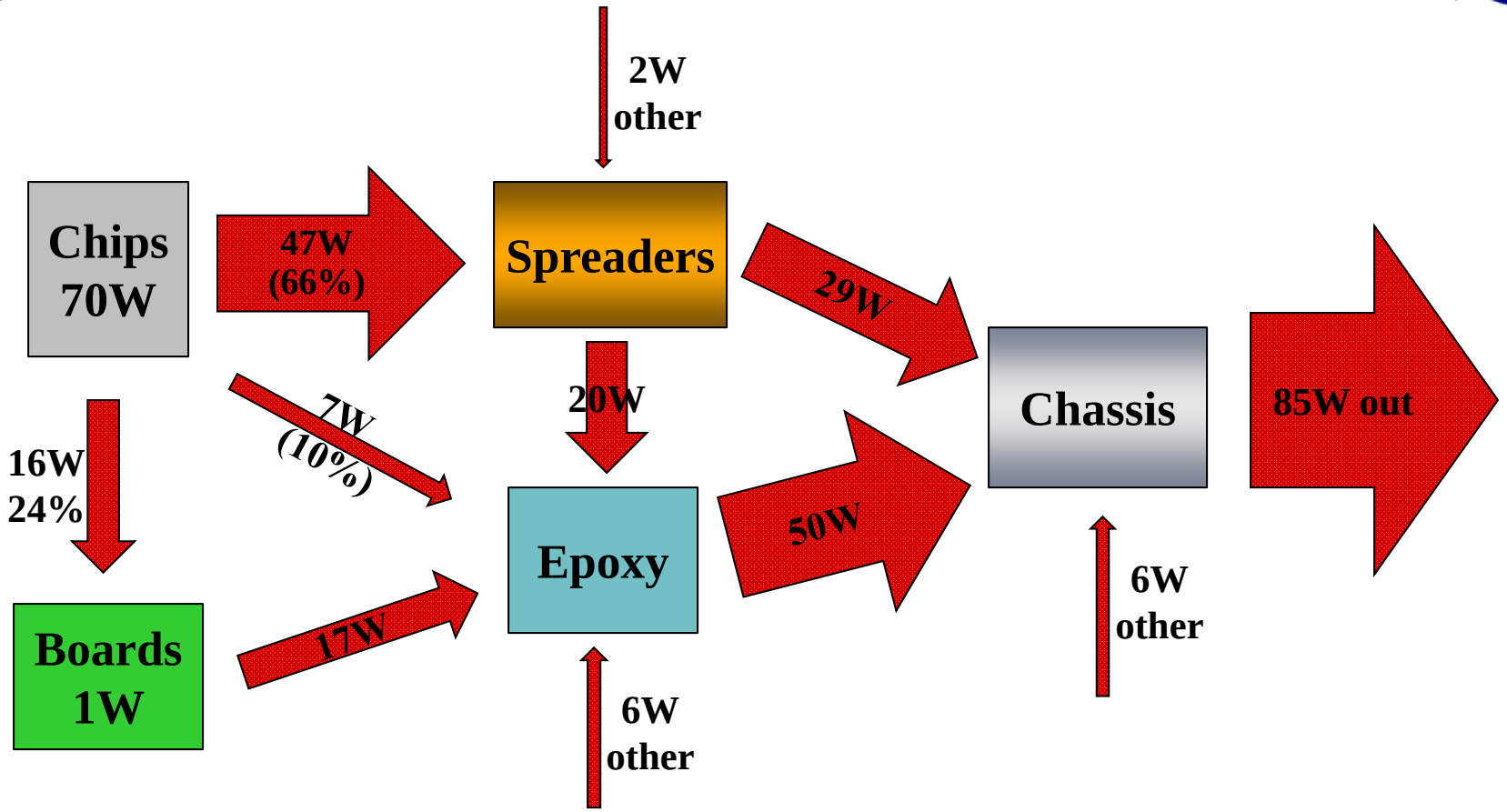
Back view

- Highest temperatures at a CPU chip and a sensor power board chip
  - Neither touches a heat spreader
- Middle boards in stack ~70°C, cooler regions ~ 60°C

Evaluation of Thermal Design

- Design incorporates both heat spreaders and thermally conductive epoxy
- How does heat flow through the system?
- What impact does each have on removal of heat?

Heat Flow Map (steady state, hot case)

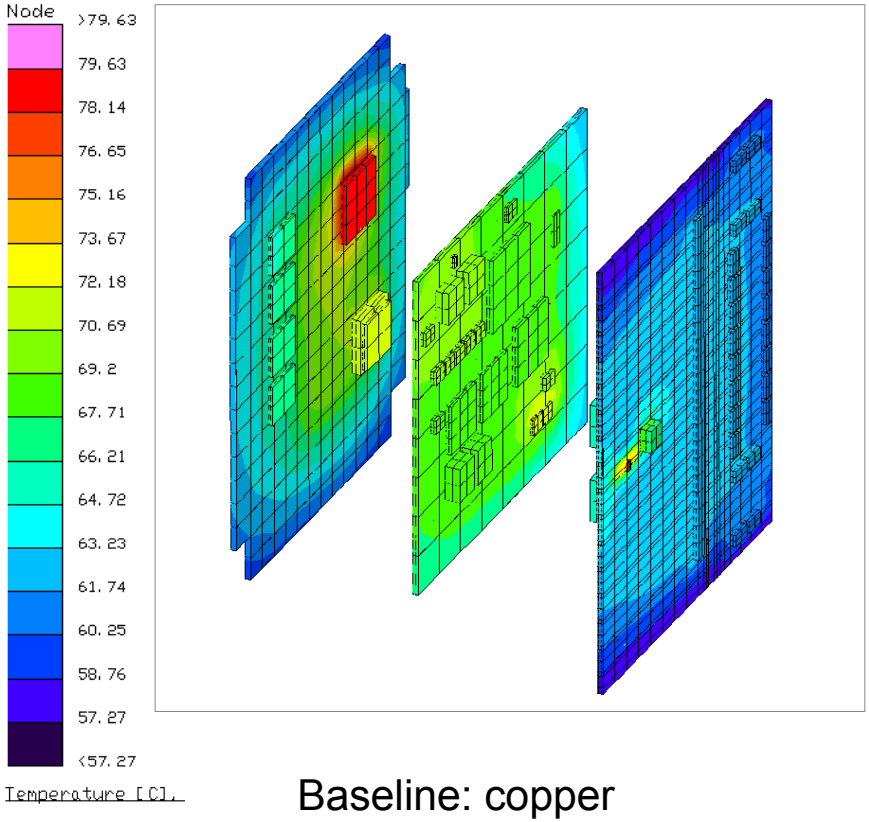


- Spreaders remove the bulk of heat from the chips
- Epoxy takes the majority of heat to the chassis
  - Lower k, but very high contact area

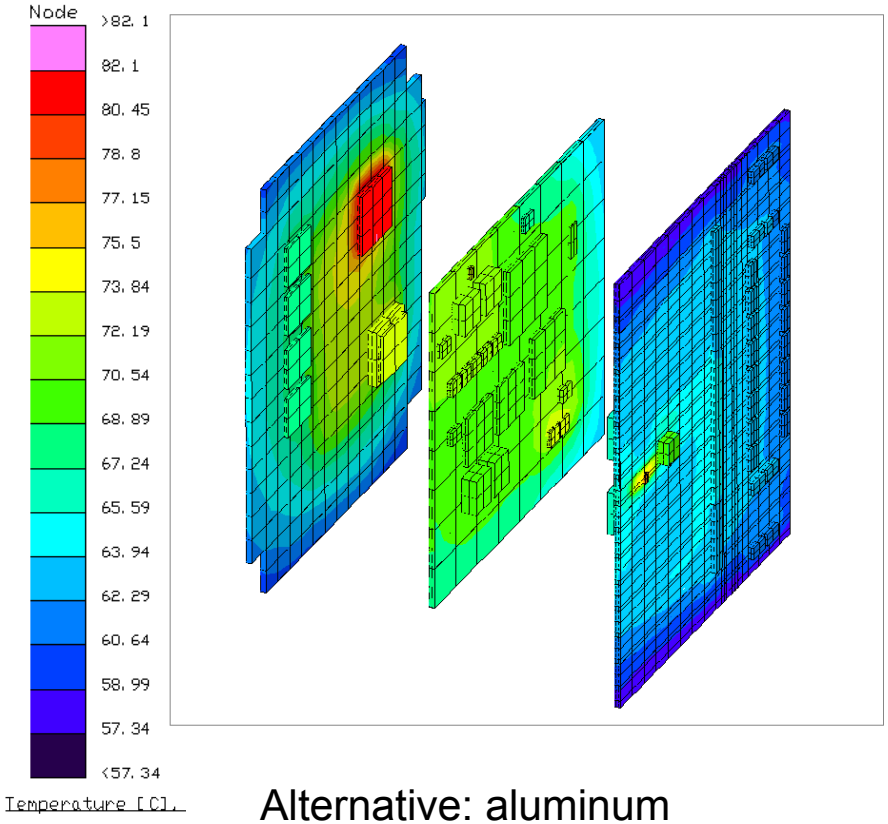
Alternative Material Simulations

- Previous simulations established a baseline
- Interest in evaluating alternative materials
- Spreader material
  - Copper
  - Aluminum
  - No spreaders (epoxy only)

Material Simulations – Spreader Material



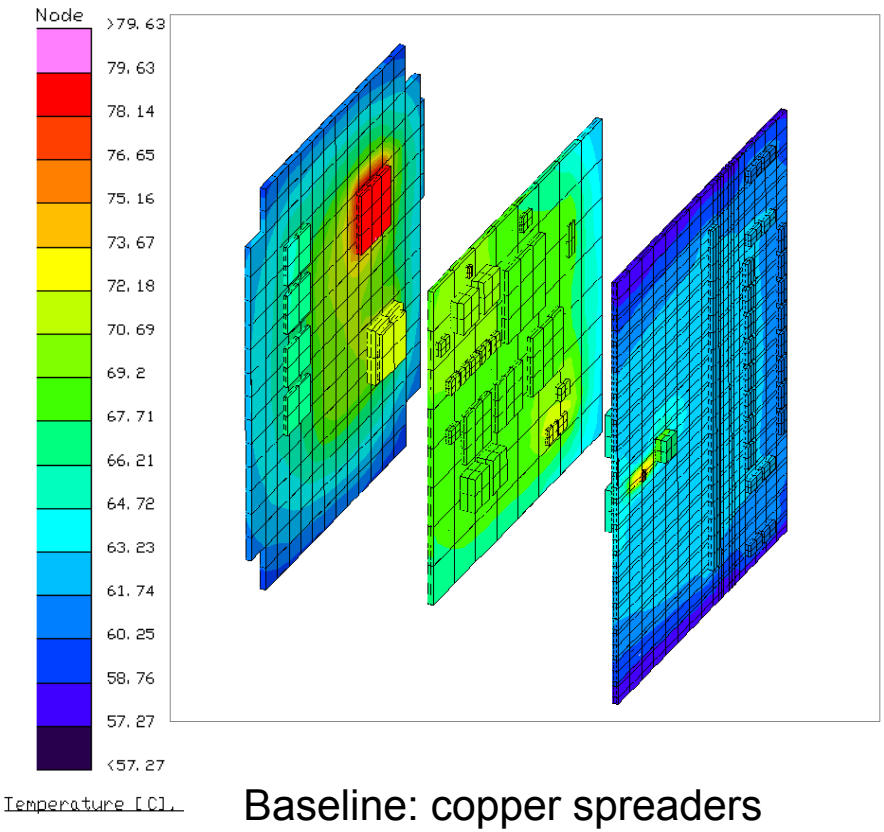
Baseline: copper



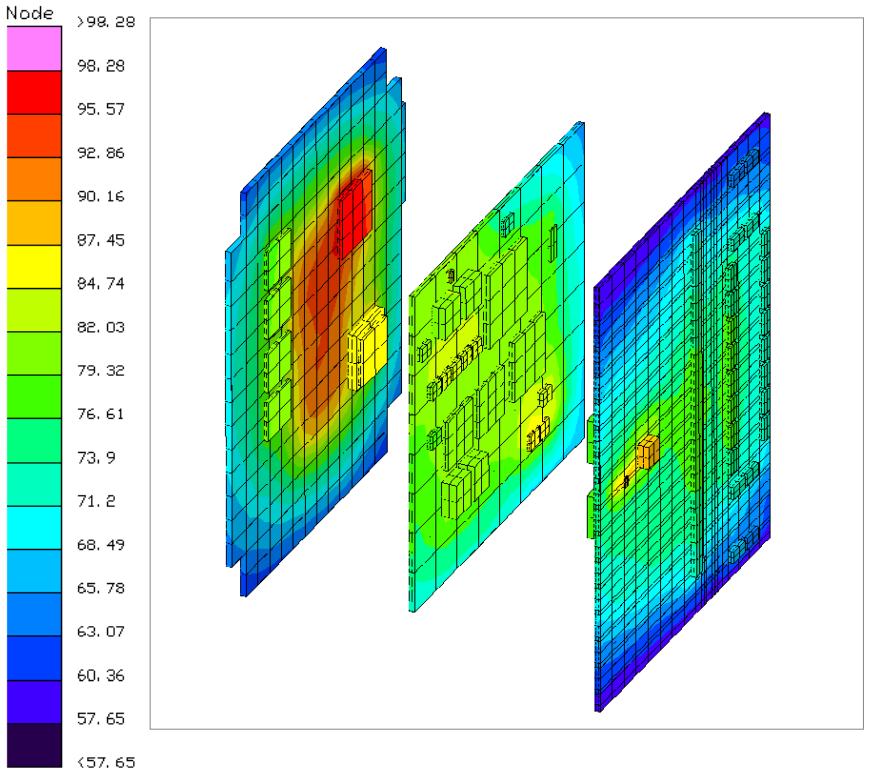
Alternative: aluminum

- Aluminum spreaders produce temperatures ≤3°C higher than copper
- Considerable weight and cost savings with aluminum

Material Simulations – Spreader Material (2)



Baseline: copper spreaders



Alternative: no spreaders (epoxy only)

- Without spreaders, peak temperatures are up to 20°C higher
  - Several components above 85°C limit
- Many areas remain cool
  - “Hot spots” are localized
- Some spreaders may not be necessary

Conclusions

- A high-detail Thermal Desktop model of HiDAQ was produced. Only minor adjustments to parameters were needed for a good correlation with test data.
- Simulations of actual operating conditions showed acceptable operating temperatures for components.
- Heat maps showed that spreaders absorb the majority of heat produced by the chips, but the epoxy ultimately delivers the most heat to the chassis.
- Simulations with alternative spreader materials showed that using aluminum instead of copper would produce only a small temperature increase of ≤3°C. This is a viable option to reduce weight and cost.
- Simulations without heat spreaders suggest that some spreaders are necessary to meet temperature limits, but others may not be essential. The design could be further optimized.

Backup Slides

Heat Load Summary

Board	Expected (W)	Op. Limits (°C)
Epoxy		-20 to +93
CPU	19.9	-40 to +85
A/D (4)	8.1 (32.4)	-40 to +85
Stack Power	8	-40 to +85
Sensor Power	13.6	-40 to +85 (175)
RFI Filter	1.2	-55 to +100
15 V Power Supply	6	-55 to +100
SSDs (2)	2 (4)	-40 to +85
Total	**85.1**	

Correlation – Steady-state Results

- Temperature results with initial estimates for parameter values
  - Results largely within 5°C of test values
  - Largest temperature deviation on one CPU chip, >10°C off
- Parametric studies showed low sensitivity to most parameters
  - Power distribution has a high impact, but is not known precisely
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6	106 <CPU Northbridge> (C)	65.1	64.4	-0.7	65.5	0.4	-0.3
7	107 <Sensor Power Board FWT> (C)	66.1	60.3	-5.8	60.8	-5.3	-0.5
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Correlation – Steady-state Results

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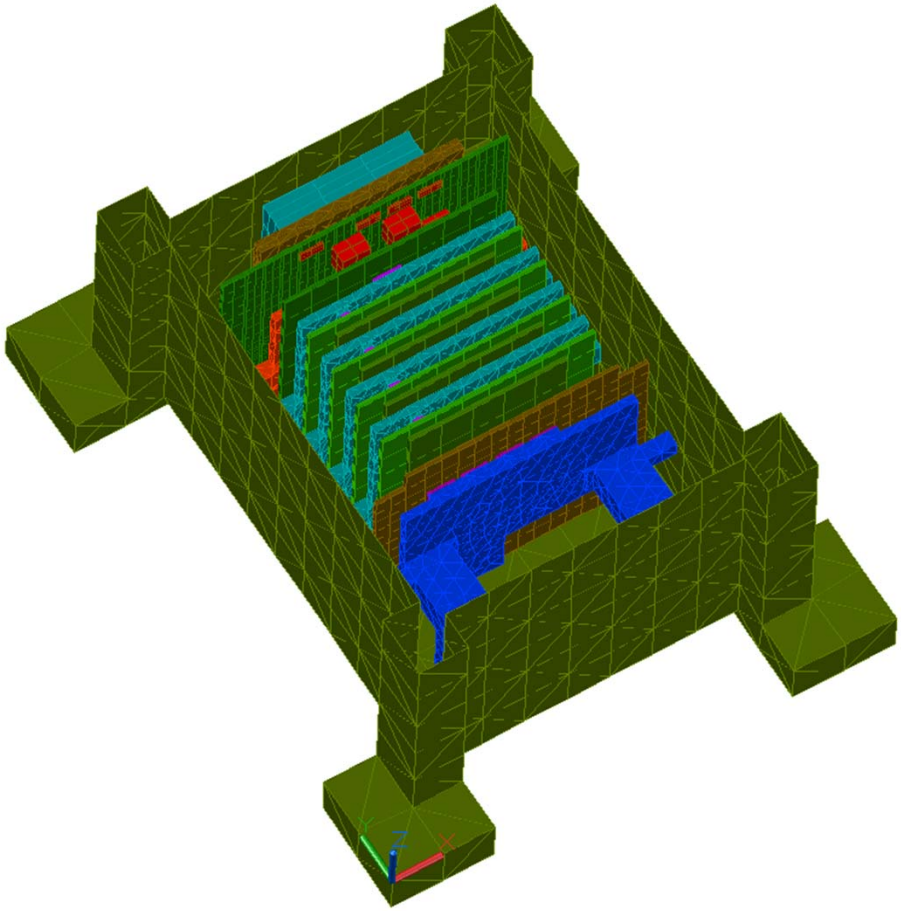
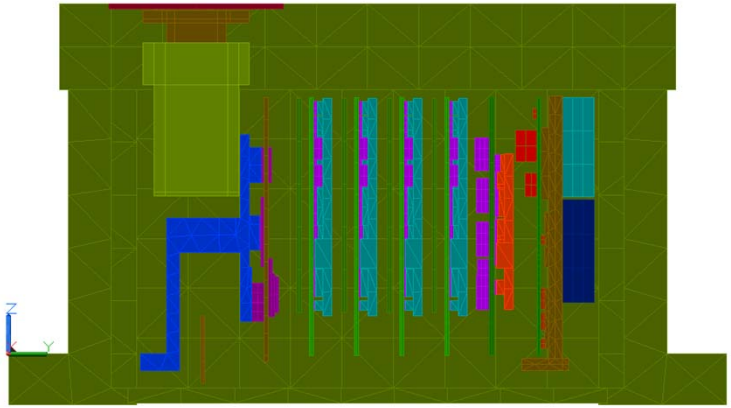
11	111 <DCDC Converter> (C)	-4.1	-3.2	0.9	-0.8	3.3	2.4

Thermal Model Discretization

- 27500 nodes
- 75000 solid elements



Isometric view (top lid hidden)



Side view with internal components