Thermal characterization of SiC MOSFET devices

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Presented By
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Outline

- Thermal transient testing of MOSFET devices
  - Potential problems with SiC
- A proposed simulation and test based method
- Experimental example
- Conclusions
Thermal transient testing of power devices

- Measure how heat is flowing through a package from junction to ambient
- Convert to a representation of the heat path as an $R_{th}$-$C_{th}$ plot (Structure Function)
- A non-destructive method to:
  - Determining $Z_{th}$
  - Providing insight to heat path segments
  - Comparing structures (e.g. to known good sample)
  - Changes over time (delamination, cracks in substrate, etc.)
  - and more…

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• The forward voltage of a PN junction under forced current condition can be used as a very accurate thermometer.

• The change of the forward voltage (TSP – temperature sensitive parameter) should be carefully calibrated against the change of the temperature (see JEDEC JESD51-1 and MIL-STD-750D).
  
  – In the calibration process the $S_{VF}$ temperature sensitivity of the forward voltage is obtained.

$$\Delta T = \Delta V_F \cdot K$$

@2mV/K sensitivity app.0.01 degC resolution can be achieved
Thermal transient test workflow

1. Find the TSP

$$y = -0.001484x + 2.725130$$

2. Calibrate

3a. Power Step

3b. Record

4. Analyze

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Each section of the Structure Function path represents physical objects the heat encounters. There is a correlation between physical objects and sections of the RC path.
• **MOS diode (Threshold mode) – current step method**
  - Gate connected to the Drain
  - The resulting two-pole device behaves as a simple diode
  - The threshold voltage can be higher than 5V

• **Heating on $R_{ds,\text{on}}$, measurement on body diode**
  - A negative sensor current is applied to the MOSFET
  - For the heating, a sufficiently high voltage is applied to the gate and the device heated with high current (IH-IS)
  - Simultaneously to the heating current switched off the gate voltage turned to zero -> the transistor closes and the sensor current flows through the diode
For SiC the second strategy may work well.

Power cycling test data on a SiC MOSFET

Separations in the structure functions indicate changes to heat flow path i.e. package structure. To better understand the cause, we align the curves based on a package component known to be reliable: MOSFET copper base-plate.

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Problems with SiC devices

• The SiO$_2$ – SiC transition, may contain trapped charge carriers due to the large concentration of crystalline errors at the interface
  – Some techniques, such as post-oxidation annealing of the gate oxide in nitric or nitrous oxide (NO or N$_2$O) may improve the device performance
• In some structures the movement of these trapped charges cause electrical disturbances up to the several seconds range after the switching
• Thermal transient tests should be carried out in connection modes, where the gate potential remains unchanged during the process.
• This makes common test procedures, such as the “MOS diode” setup and the fixed $V_{DS}$ arrangement unsuitable for testing SiC devices.
Examples of electrical parasitic response

- SiC MOSFET measured with 20A sensor current, 240 A heating current and 15V $V_{GS}$

Strong non-monotonous behavior, even at larger time constants
Examples of electrical parasitic response

- SiC MOSFET measured with 20A sensor current, 5A heating current and 10V VGS

No ideal fit if dual-interface technique is used – not pure thermal signal
Measuring the reverse diode always works

• As the issues demonstrated above most likely correspond to a gate charge related phenomena, the SiC diodes are not affected

Separation is of pure thermal origin
Proposed method

- Measuring the diode only is not enough – transistor characteristics is also necessary
  1. Use diode test data to calibrate the simulation model of the component
  2. Get the transistor thermal properties from the calibrated simulation model
Detailed Model Calibration

- Build detailed model of the component
- Adjust material properties and geometries until the simulated thermal response matches the measurement
- Achieved via an automated optimization process

Calibrated – End of 1st Pulse

Best Guess – End of 1st Pulse

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EXPERIMENTAL
Test arrangement and simulation model

- Use a Si IGBT package with embedded reverse diodes as demonstrator
- This allows not only simulation but experimental verification as well – may not be possible in case of SiC module
Comparison of test and simulation

• First simulation attempt – similar shape, but multiple inaccuracies
Optimization of simulation parameters I.

• Main variables are
  – Thermal conductivity coefficients
  – Size of package features
  – Specific heat and density (less important)

• Set up simulation scenarios

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Initial Value</th>
<th>Parameter range</th>
<th>Calibrated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Area</td>
<td>mm²</td>
<td>81</td>
<td>64 ~ 81</td>
<td>79</td>
</tr>
<tr>
<td>Die Adhesive</td>
<td>W/mK</td>
<td>33</td>
<td>30 ~ 35</td>
<td>33</td>
</tr>
<tr>
<td>Ceramic</td>
<td>W/mK</td>
<td>25</td>
<td>25 ~ 35</td>
<td>34</td>
</tr>
<tr>
<td>Solder</td>
<td>W/mK</td>
<td>40</td>
<td>35 ~ 45</td>
<td>45</td>
</tr>
</tbody>
</table>

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Cross-verification

• Very good match as the DA layer and the substrate is already calibrated

• From here the package thermal metrics can be identified accurately using simulation
Determining $R_{thJC}$ from model

- $R_{thJC}$ can be determined based on its definition.
  - We used two possible interpretations:
    - $R_{thJC} = \frac{T_j(max) - T_C(max)}{dP}$
    - $R_{thJC} = \frac{T_j(mean) - T_C(mean)}{dP}$

Case region

Junction regions

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Comparison of simulation data to test

- The divergence separation region of the structure functions is in line with the $R_{thJC}$ range calculated based on the model.

<table>
<thead>
<tr>
<th>Temperatures</th>
<th>Maximum</th>
<th>Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base plate [°C]</td>
<td>70.3373</td>
<td>62.9045</td>
</tr>
<tr>
<td>IGBT active area [°C]</td>
<td>75.829</td>
<td>74.2957</td>
</tr>
<tr>
<td>$R_{thJC}$ [K/W]</td>
<td>0.079</td>
<td>0.163</td>
</tr>
</tbody>
</table>

$dP=69.5W$
Conclusions

- Thermal transient testing using electrical test methods can be applied to SiC semiconductors package thermal characterization.
- Certain novel compound semiconductor structures require non-standard test methods or in particular cases may not be suited to this characterization method.
- The reverse diode, if present is a well measurable component.
- Based on the thermal transient response of this component the package structure can be identified.
- If a thermal simulation environment is available, the simulation model can be calibrated to the test-based structure functions.
  - The calibrated model will respond correctly in a wide range of time constants.
- Using this calibrated model the thermal properties of all heat sources in the package can be simulated.
- Having a calibrated package model has further benefits, it helps to identify a suitable way to interpret the separation point of structure functions if the separation is not a clear single point, but shows up rather like a continuous region.

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